UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,321	01/18/2002	Santosh C. Lolayekar	E003 - 1000US1	7045

48789 7590 11/27/2007

LAW OFFICES OF BARRY N. YOUNG
260 SHERIDAN AVENUE
SUITE 410
PALO ALTO, CA 94306-2047

EXAMINER	
REFAI, RAMSEY	

ART UNIT	PAPER NUMBER
3627	

MAIL DATE	DELIVERY MODE
11/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/051,321
Filing Date: January 18, 2002
Appellant(s): LOLAYEKAR ET AL.

Barry Young
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed August 24, 2007 appealing from the Office action mailed December 20, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,400,730	Latif et al	6-2002
6,693,906	Tzeng	2-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 8-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Latif et al (U.S. Patent No. 6,400,730) in view of Tzeng (U.S. Patent No. 6,693,906).

3. As per claim 1, Latif et al disclose a switch for use in a network, comprising:

a plurality of linecards, each including: a plurality of ports; and a plurality of storage protocol processing units, wherein each storage protocol processing unit is associated with at least one port and performs storage command processing for commands received at said at least one port, thereby distributing processing resources amongst linecard ports **(column 2, line 55-column 3, line 21, column 7, lines 46-column 8, line 15)**

Latif et al disclose the processing of storage commands **(column 1, lines 25-30, column 6, lines 9-10, column 19, lines 30-37,)** but fail to explicitly disclose that the switch processes packets without buffering the packets . However, Tzeng discloses a network switch that processes incoming data packets without buffering **(column 1, line 39-column 2, lines 16).** It would have been obvious to one of the ordinary skill in the art at the time of the Applicant's invention to combine the teachings of Latif et al and Tzeng because doing so would reduce the overall cost of the network switch and enhance switching performance.

4. As per claim 2, Latif et al disclose wherein additional linecards can be added to the plurality of linecards **(Fig. 5, column 7, lines 25-67).**

5. As per claim 3, Latif et al disclose wherein linecards can be removed from the plurality of linecards **(Fig 5).**

6. As per claim 4, Latif et al disclose wherein each linecard is designed to handle packets formatted in accordance with any respective one of a plurality of protocols **(column 2, lines 15-67).**

7. As per claim 5, Latif et al disclose wherein: a first set of linecards in the plurality is designed to end and receive packets in accordance with an iSCSI protocol; and a second set of linecards in the plurality is designed to send and receive packets in accordance with a Fibre Channel protocol **(column 2, lines 15-67).**

8. As per claim 6, Latif et al disclose wherein one of the plurality of protocols is Infiniband **(column 4, line 16).**

9. As per claim 8, Latif et al fail to explicitly disclose wherein the switch is capable of processing packets at wire speed. However, Tzeng discloses a network switch that processes incoming data packets without buffering to ensure that switches have switching capabilities for faster speed networks such as 100Mbps or gigabit networks **(column 1, line 39-column 2, lines 16).** It would have been obvious to one of the ordinary skill in the art at the time of the Applicant's invention to combine the teachings of Latif et al and Tzeng because doing so reduce the overall cost of the network switch and enhance switching performance.

10. As per claim 9, Latif et al disclose wherein the switch is capable of receiving a packet at a first port of a first linecard destined for a virtual target and formatted in accordance with a first protocol **(column 2, lines 34-column 3, line 22)**, determining if the packet is a data or control packet **(column 7, lines 49-59)**, and if the packet is a data packet, sending the packet formatted in accordance with a second protocol to a physical target **(column 2, lines 34-column 3, line 22)**. Latif et al fail to explicitly disclose it's all without buffering the packets. However, Tzeng discloses a network switch that processes incoming data packets without buffering **(column 1, line 39-column 2, lines 16).** It would have been obvious to one of the ordinary skill in the art at the time of the Applicant's invention to combine the teachings of Latif et al and Tzeng because doing so would reduce the overall cost of the network switch and enhance switching performance.

11. As per claim 10, Latif et al disclose wherein the switch is capable of receiving a packet at a first port of a first linecard destined for a virtual target and formatted in accordance with a first protocol, determining if the packet is a data or control packet, and if the packet is a data packet, sending the packet formatted in accordance with a second protocol to a physical target **(column 2, lines 34-column 3, line 22)**. Latif et al fail to explicitly disclose wherein the switch is capable of processing packets at wire speed. However, Tzeng discloses a network switch that processes incoming data packets without buffering to ensure that switches have switching capabilities for faster speed networks such as 100Mbps or gigabit networks **(column 1, line 39-column 2, lines 16).** It would have been obvious to one of the ordinary skill in the art at the time of the Applicant's invention to combine the teachings of Latif et al and Tzeng because doing so reduce the overall cost of the network switch and enhance switching performance.

12. As per claim 11, Latif et al disclose wherein the switch is capable of performing a storage service at the request of a second device without any additional involvement of the second device **(column 1, lines 18-35)**.

13. As per claim 12, Latif et al disclose wherein the second device is a server **(column 1, lines 18-35)**.

14. As per claim 13, Latif et al disclose wherein the second device is a management station **(column 1, lines 18-35)**.

15. As per claim 14, Latif et al disclose wherein the storage service is any one of local mirroring, mirroring over slow link, snapshot, replication, third-party copy, periodic backup, and restore **(column 1, lines 25-40)**.

16. As per claim 15, Latif et al disclose a switch for use in a network, comprising: a plurality of linecards, each linecard including: a plurality of ports; a plurality of processing units, wherein each processing unit is associated with at least one port and is associated, with a memory; a CPU in communication with the processing units; and a fabric in communication with each linecard, thereby allowing packets to pass from an ingress linecard to an egress linecard **(Fig. 15, column 2, line 55-column 3, line 21, column 7, lines 46-column 8, line 15).**

Latif et al disclose the processing of storage commands **(column 1, lines 25-30, column 6, lines 9-10, column 19, lines 30-37,)** but fail to explicitly disclose that the switch processes packets without buffering the packets. However, Tzeng discloses a network switch that processes incoming data packets without buffering **(column 1, line 39-column 2, lines 16).** It would have been obvious to one of the ordinary skill in the art at the time of the Applicant's invention to combine the teachings of Latif et al and Tzeng because doing so would reduce the overall cost of the network switch and enhance switching performance.

17. As per claim 16, Latif et al disclose wherein: each processing unit includes a packet aggregation and classification unit and a packet-processing unit; and the associated memory includes a CAM and an SRAM **(column 7, line 45-column 8, line 15, Figs, 8, 16-17)**.

18. As per claim 17, Latif et al disclose wherein the associated memory is included in the processing unit **(Figs, 8, 16-17)**.

19. As per claim 18, Latif et al disclose wherein the associated memory is associated with each processing unit **(Figs, 8, 16-17)**.

20. As per claim 19, Latif et al disclose wherein the switch further includes a traffic manager in communication with each processing unit **(column 7, line 45-column 8, line 15)**.

21. As per claim 27-28, Latif et al discloses virtualization **(see column 11, lines 5-30, column 16, lines 30-42, column 7, lines 26-46; address translation).**

22. As per claims 20-26 and 29-44, these claims contain similar limitations as claims 1-6, 8-19 and 27-28 above, therefore are rejected under the same rationale.

(10) Response to Argument

Appellant is reminded that claims must be given their broadest reasonable interpretation consistent with the specification (MPEP ch. 2111) and that a prior art reference must be considered in its entirety (MPEP ch. 2142.02).

- **Argument A:** *Latif et al and Tzeng cannot be combined as proposed. The combination of Latif et al and Tzeng would not render the claimed invention predictable. The combination cannot be combined as proposed.*

The Examiner respectfully disagrees. It is noted that KSR forecloses the argument that a **specific** teaching, suggestion, or motivation is required to support a finding of obviousness. See the recent Board decision *Ex parte Smith*, --USPQ2d--, slip op. at 20, (Bd. Pat. App. & Interf. June 25, 2007) (citing *KSR*, 82 USPQ2d at 1396).

Nonetheless, Examiner asserts that Latif et al and Tzeng are in the same field of endeavor and are thus combinable. Both are directed to the transferring and routing of data packets in a network. The Appellant argues that "*Tzeng's 'suggestion' of no buffering is incompatible with Latif's requirement for buffering*" (page 18 of Brief) and "*Latif et al explicitly teaches that buffering is a necessary feature if his disclosed switching and routing apparatus and process*" (page 13 of Brief). The Examiner disagrees with the argument that the buffer is a necessary and crucial feature in Latif's method of switching and routing packets. In **column 9, lines 48-57**, Latif et al discloses that the Buffer to Buffer receive data field is used to *force end nodes to communicate with data frames that will fit within the IP packet carried over an Ethernet link.* The buffer-to-buffer data field is used to control the size of the data frame. One skilled in the art would recognize that Latif's system would remain functional and operative without the Buffer to Buffer receive data field for packets that do not exceed the maximum allowed size. The system would not be rendered inoperative without the use of the buffer-to-buffer data field.

Latif et al further discloses in **column 15, lines 14-16** that "*it is necessary to buffer the entire frame to determine the length and checksum and write them into the header*." Here, Latif et al buffers the data frame to determine the length and checksum from the frame. One skilled in the art would appreciate that this step would not render Latif's system inoperative since the buffering is used to determine the length and checksum from the data frame. One skilled in the art would also recognize that Latif's system would remain functional and operative without determining the length and checksum for packets that do not exceed the maximum allowed size. In other words, Latif's system without buffering would still work for packets or data frames that do not exceed the maximum size.

Furthermore, determining the checksum is a step performed as a redundancy check to protect the integrity of data. The lack of this step would certainly not render Latif's system inoperative.

Latif's system therefore would not be rendered inoperative without buffering. Since Latif et al and Tzeng are both directed to the transferring and routing of data packets in a network, the combination of Latif et al and Tzeng is combinable. Latif et al et al disclose the processing of storage commands **(column 1, lines 25-30, column 6, lines 9-10, column 19, lines 30-37)** but fail to explicitly disclose that the switch processes packets without buffering the packets. However, Tzeng discloses a network switch that processes incoming data packets without buffering **(column 1, line 39-column 2, lines 16).** It would have been obvious to one of the ordinary skill in the art at the time of the Appellant's invention to combine the teachings of Latif et al and Tzeng because doing so would reduce the overall cost of the network switch and enhance switching performance.

- **Argument B:** *Tzeng does not disclose switching of packets without buffering or at wire speed. Latif et al and Tzeng do not disclose nor suggest that the switch, network, or method operates to perform the particular type of packet claimed in each claim either "without buffering" or "at wire speed". The references do not disclose or suggest wire speed*

In response, the Examiner respectfully disagrees. Wire speed, as noted by the Appellant on pages 22-23 of the Brief, means that the packets are processed *without buffering.* Tzeng clearly discloses processing packets at a switch without buffering or at the same rate that the data packets are received at the switch **(See column 1, line 39-column 2, lines 16).** Furthermore, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See/n *re Keller,* 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Therefore, the combination of Latif et al and Tzeng meet the scope of the claimed limitation.

- **Argument C:** *Latif et al does not disclose or suggest a storage service comprising one of local mirroring, mirroring over a slow link, snapshot, replication, third-party copy, periodic backup, and restore as set out in claim 14.*

In response, the Examiner respectfully disagrees. Latif et al disclose storage services such as third party copy **(column 12, lines 60-67)** and data backup **(column 16, lines 15-17, column 1, lines 25-35).** Therefore the combination of Latif et al and Tzeng meet the scope of the claimed limitation

- **Argument D:** Latif et al and Tzeng fail to disclose a plurality of processing units each of which includes a classifier, a virtualizer, and a translator that classifies, virtualizes and translates packets.

In response, the Examiner respectfully disagrees. Latif et al discloses that the switch performs translation of data packets between SCSi, Fibre Channel and Ethernet devices. **(column 1, lines 18-25, column 3, lines 5-21, column 6, lines 44-57).** Latif et al further discloses that the switch performs address translation (virtualization) **(see column 11, lines 5-30, column 16, lines 30-42, column 7, lines 26-46).** Tzeng et al discloses a packet classifier **(see column 3, lines 35-45).** Therefore the combination of Latif et al and Tzeng meet the scope of the claimed limitation.

- **Argument E:** *Latif et al and Tzeng fail to disclose or suggest means for performing wire speed storage command processing of packets.*

In response, the Examiner respectfully disagrees. Latif et al et al disclose the processing of storage commands **(column 1, lines 25-30, column 6, lines 9-10, column 19, lines 30-37,)** but fail to explicitly disclose that the switch processes packets at wire speed . However, Tzeng discloses a network switch that processes incoming data packets without buffering **(column 1, line 39-column 2, lines 16).** It would have been obvious to one of the ordinary skill in the art at the time of the Appellant's invention to combine the teachings of Latif et al and Tzeng because doing so would reduce the overall cost of the network switch and enhance switching performance. Therefore the combination of Latif et al and Tzeng meet the scope of the claimed limitation.

- **Argument F:** *The Office failed to properly construe Claim 21 in accordance with 35 USC 112-6th paragraph.*

In response, the Examiner respectfully disagrees. **It is first noted that claim 21 is a single means claim.** MPEP sec 2181-V entitled "SINGLE MEANS CLAIMS" recites:

"Donaldson does not affect the holding of In re Hyatt, 708 F.2d 712, 218 USPQ 195 (Fed. Cir. 1983) to the effect that ***a single means claim does not comply with the enablement requirement of 35 U.S.C. 112, first***

paragraph. As Donaldson applies only to an interpretation of a limitation drafted to correspond to 35 U.S.C. 112, sixth paragraph, which by its terms is limited to "an element in a claim to a combination," ***it does not affect a limitation in a claim which is not directed to a combination***."

Furthermore, one skilled in the art would not be able to recognize the corresponding structure of the means plus function from the Appellant's disclosure without the aid of the Appellant. MPEP sec. 2181-I states:

"The USPTO must apply 35 U.S.C. 112, sixth paragraph in appropriate cases, and **give claims their broadest reasonable interpretation, in light of and *consistent with the written description of the invention in the application.*** See Donaldson, 16 F.3d at 1194, 29 USPQ2d at 1850 (stating that 35 U.S.C. 112, sixth paragraph "merely sets a limit on how broadly the PTO may construe means-plus-function language under the rubric of reasonable interpretation.'")."

Further, MPEP sec. 2181-II states:

"35 U.S.C. 112, sixth paragraph states that a claim limitation expressed in means-plus-function language "shall be construed to cover the corresponding structure…described in the specification and equivalents thereof." "***If one employs means plus function language in a claim, one must set forth in the specification an adequate disclosure showing what is meant by that language.*** If an applicant fails to set forth an adequate disclosure, the applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112." In re Donaldson Co., 16 F.3d 1189, 1195, 29 USPQ2d 1845, 1850 (Fed. Cir. 1994) (in banc). The proper test for meeting the definiteness requirement is that the ***corresponding structure (or material or acts) of a means (or step)-plus-function limitation must be disclosed in the specification itself in a way that one skilled in the art will understand what structure (or material or acts) will perform the recited function***."

The Appellant has not set forth an adequate disclosure describing the corresponding structure of the means plus function. One skilled in the art would not be able to clearly locate and recognize the corresponding structure of the means plus function. The Examiner has given the means plus function in claim 21 the broadest reasonable interpretation consistent with the specification as best understood. Throughout prosecution, the Appellant has not referenced the corresponding structure of the means plus function. However, in the Summary of Claimed Subject Matter section of the Brief, the Appellant now references the corresponding structure of the means plus function as follows:

"means **[701, Fig. 7; pg.17, lns. 11-15]** associated with each port for performing wire speed storage command processing of packets **[specification pg. 6, lns. 15-2; pg. 13, lns. 12-16]"**

The following are the cited sections above:

- **Page 17, lines 11-15:**

[Storage Processor Unit. In one embodiment, each port is associated with a Storage Processor Unit (SPU) 701. The SPU rapidly processes the data traffic allowing for wire-speed operations. In one embodiment, the SPU includes several elements: a Packet Aggregation and Classification Engine (PACE) 704, a Packet Processing Unit (PPU) 706, an SRAM 705, and a CAM 707. Still]

- **Page 6, lines 15-2? (typo will be taken as lines 15-20):**

[Further, a storage switch in accordance with the invention allows a multi-protocol SAN, e.g., one that includes both iSCSI (a recently introduced protocol carried over an Ethernet connection) or Fibre Channel, and to process any data packets at "wire speed" - that is, without introducing any more latency that would be introduced by a switch that merely performed switching or routing functions - and thus a switch in accordance with the invention has a high bandwidth. Typically to process data]

- **Page 13, lines 12-16:**

[Further, the distributed intelligence allows a switch in accordance with an embodiment of the invention to process data at "wire speed," meaning that a storage switch 304 introduces no more latency to a data packet than would be introduced by a typical network switch (such as switch 112 in Fig. 1). Thus, "wire speed" for the switch is measured by the connection to the particular port.]

The Examiner asserts that one skilled in the art would not be able to recognize the above citations as being the corresponding structure for the means plus function of claim 21 with the Appellant's assistance.

Latif et al and Tzeng do disclose the corresponding structure as understood from the above citations. Latif et al disclose a plurality of storage protocol processing units, wherein each storage protocol processing unit is associated with at least one port and performs storage command processing for commands received at said at least

one port, thereby distributing processing resources amongst linecard ports **(column 2, line 55-column 3, line 21, column 7, lines 46-column 8, line 15).** Latif et al disclose the processing of storage commands **(column 1, lines 25-30, column 6, lines 9-10, column 19, lines 30-37)** but fail to explicitly disclose that the switch processes packets without buffering the packets. However, Tzeng discloses a network switch that processes incoming data packets without buffering **(column 1, line 39-column 2, lines 16).** It would have been obvious to one of the ordinary skill in the art at the time of the Applicant's invention to combine the teachings of Latif et al and Tzeng because doing so would reduce the overall cost of the network switch and enhance switching performance. Furthermore, Latif et al discloses a Packet Aggregation and Classification Engine and a Packet Processing Unit. Latif et al disclose that the switch performs translation of data packets between SCSi, Fibre Channel and Ethernet devices. **(column 1, lines 18-25, column 3, lines 5-21, column 6, lines 44-57).** Latif et al further discloses that the switch performs address translation (virtualization) **(see column 11, lines 5-30, column 16, lines 30-42, column 7, lines 26-46).** Tzeng et al discloses a packet classifier **(see column 3, lines 35-45).**

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Ramsey Refai/

Examiner, Art Unit 3627

Conferees:

*/F. Ryan Zeender/

Supervisory Patent Examiner, Art Unit 3627

*/Michael Cuff/ for Vincent Millin

Primary Examiner, Art Unit 3627